Listing of Claims:

1. (currently amended) A pulse width modulation regulator, comprising:

a charge pump;

a comparator circuit coupled to the charge pump, the comparator circuit for providing an output voltage; and

a latch circuit coupled to the charge pump for ensuring that the charge pump is adjusted such that an undershoot condition and an overshoot condition of the output voltage is minimized, wherein the latch circuit comprises:

a first SR latch,

a second SR latch, wherein an input of the second SR latch comprises the output voltage,

a first gate, wherein an input of the first gate comprises an output from the second SR latch and an input signal, wherein an output of the first gate comprises a first signal to the charge pump, wherein the first signal prevents the overshoot condition, and

a second gate, wherein an input of the second gate comprises an output from the first SR latch and the input signal, wherein an output of the second gate comprises a second signal to the charge pump, wherein the second signal prevents the undershoot condition.

2. (original) The regulator of claim 1, wherein an input of the comparator circuit comprises an output of the charge pump.

3. (original) The regulator of claim 1, wherein an input of the latch circuit comprises the output voltage.

4. (original) The regulator of claim 3, wherein the latch circuit transmits a first signal to the charge pump when the output voltage is in a first state, wherein the first signal prevents the overshoot condition.

5. (original) The regulator of claim 4, wherein the first signal prevents the output of the charge pump from increasing further.

6. (original) The regulator of claim 4, wherein in the first state, the output voltage goes high during a clock cycle.

7. (original) The regulator of claim 3, wherein the latch circuit transmits a second signal to the charge pump when the output voltage is in a second state, wherein the second signal prevents the undershoot condition.

8. (original) The regulator of claim 7, wherein the second signal prevents the output of the charge pump from decreasing further.

9. (original) The regulator of claim 7, wherein in the second state, the output voltage goes low during a clock cycle.

10. (canceled)

11. (currently amended) The regulator of claim ~~10~~ 1, wherein the latch circuit further comprises:

a first D flip-flop coupled between the first SR latch and the second gate; and

a second D flip-flop coupled between the second SR latch and the first gate.

12. (original) The regulator of claim 1, wherein the comparator circuit comprises:

a clock circuit; and

an inverter coupled to an output of the clock circuit.

13. (original) The regulator of claim 1, wherein the comparator circuit comprises:

a clock circuit; and

a pulse generator coupled to an input of the clock circuit.

14. (currently amended) A pulse width modulation regulator, comprising:

a charge pump;

a voltage comparator circuit, wherein an input of the voltage comparator circuit comprises an output of the charge pump; and

a latch circuit, wherein an input of the latch circuit comprises an output from the voltage comparator circuit,

wherein the latch circuit transmits a first signal to the charge pump when the output from the voltage comparator circuit is in a first state, wherein the first signal prevents an overshoot of a desired output voltage,

wherein the latch circuit transmits a second signal to the charge pump when the output from the voltage comparator circuit is in a second state, wherein the second signal prevents an undershoot of the desired output voltage

wherein the latch circuit comprises:

a first SR latch,

a second SR latch, wherein an input of the second SR latch comprises the output signal from the voltage comparator circuit,

a first gate, wherein an input of the first gate comprises an output from the first SR latch and an input signal, wherein an output of the first gate comprises the second signal, and

a second gate, wherein an input of the second gate comprises an output from the second SR latch and the input signal, wherein an output of the second gate comprises the first signal.

15. (original) The regulator of claim 14, wherein the transmission of the first signal prevents the output of the charge pump from increasing further.

16. (original) The regulator of claim 14, wherein the transmission of the second signal prevents the output of the charge pump from decreasing further.

17. (canceled)

18. (currently amended) The regulator of claim ~~17~~ 14, wherein the latch circuit further comprises:

a first D flip-flop coupled between the first SR latch and the first gate; and

a second D flip-flop coupled between the second SR latch and the second gate.

19. (original) The regulator of claim 14, wherein in the first state, the output signal

from the voltage comparator circuit goes high during a clock cycle.

20. (original) The regulator of claim 14, wherein in the second state, the output signal from the voltage comparator circuit goes low during a clock cycle.

21. (original) The regulator of claim 14, wherein the voltage comparator circuit comprises:

a clock circuit; and

an inverter coupled to an output of the clock circuit.

22. (original) The regulator of claim 14, wherein the voltage comparator circuit comprises:

a clock circuit; and

a pulse generator coupled to an input of the clock circuit.

23. (original) A pulse width modulation regulator, comprising:

a charge pump;

a voltage comparator circuit, wherein an input of the voltage comparator circuit comprises an output of the charge pump; and

a latch circuit, comprising:

a first SR latch,

a second SR latch, wherein an input of the second SR latch comprises an output from the voltage comparator circuit,

a first gate, wherein an input of the first gate comprises an output from the first

SR latch and an input signal, wherein the first gate transmits a first signal to the charge pump when the output from the voltage comparator circuit is in a first state, wherein the first signal prevents the output from the charge pump from increasing further, and

a second gate, wherein an input of the second gate comprises an output from the second SR latch and the input signal, wherein the second gate transmits a second signal to the charge pump when the output from the voltage comparator circuit is in a second state, wherein the second signal prevents the output from the charge pump from decreasing further.

24. (original) The regulator of claim 23, wherein the latch circuit further comprises:

a first D flip-flop coupled between the first SR latch and the first gate; and

a second D flip-flop coupled between the second SR latch and the second gate.

25. (Withdrawn)

26. (Withdrawn)

27. (Withdrawn)\

28. (Withdrawn)

29. (Withdrawn)

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32. (Withdrawn)

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35. (Withdrawn)

36. (Withdrawn